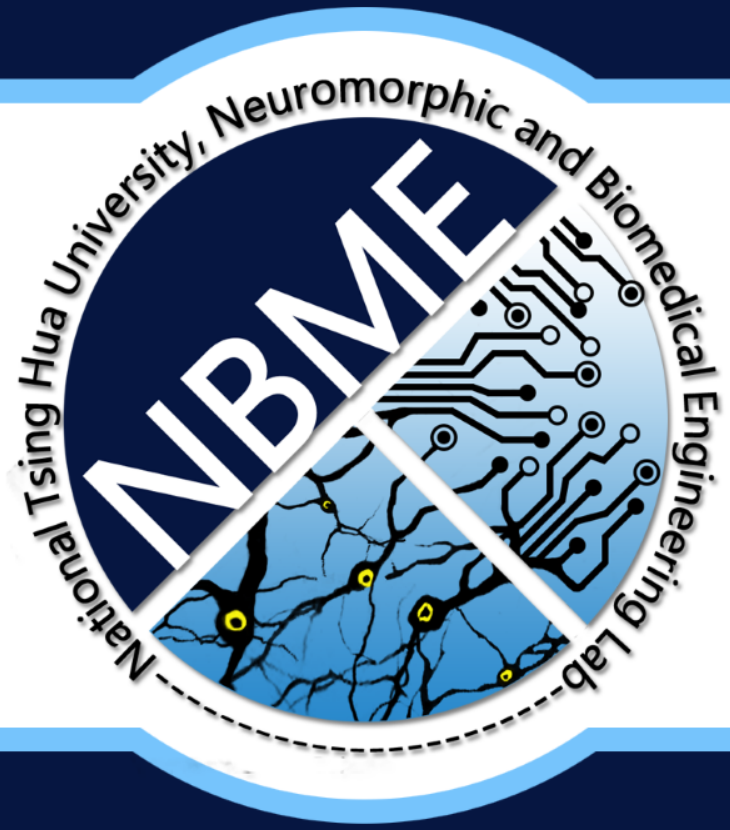

實作專題介紹

鄭桂忠老師

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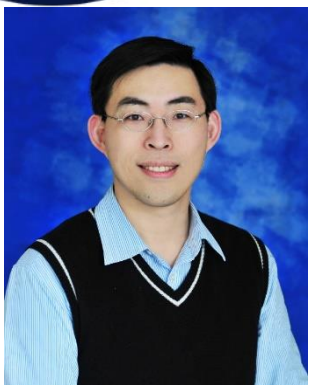
仿生與生醫工程研究室



鄭桂忠 教授

Kea-Tiong (Samuel) Tang

Professor

Vice President, IEEE CASS

Past Chair, IEEE Taipei Section

Editor-in-Chief, TBioCAS

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Research Interests

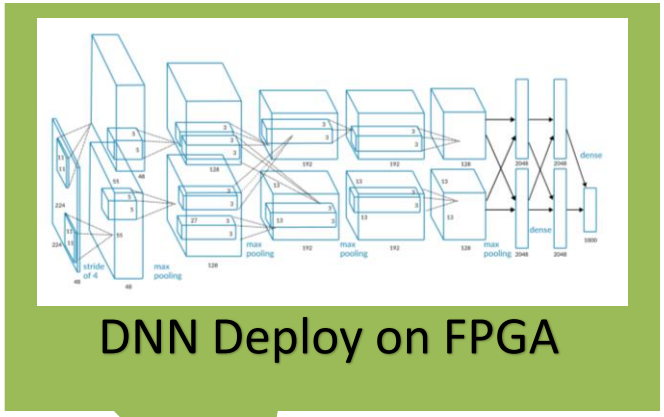
- 仿神經人工智慧晶片 (系統A組+系統B組)
  Neuromorphic AI chip
- 電子鼻系統 (系統A組+系統B組)
  Miniature Electronic Nose System
- 生醫晶片與系統-醫用植入、腦機介面、神經輔具 (系統A組+系統B組)
  Medical implant, brain-machine interface, neural prosthesis
- 演算法、信號處理、類比電路、系統晶片 (系統A組+系統B組)
  Algorithm, Signal processing, Analog circuit, System-on-chip

專題題目

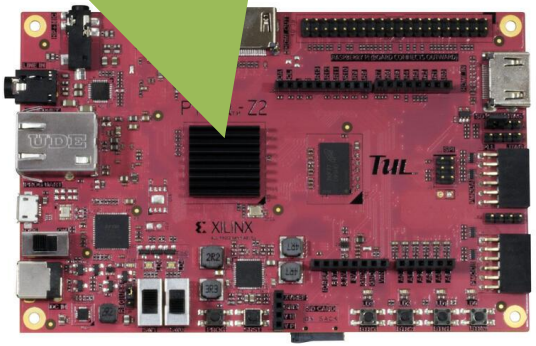
- 數位電路專題：
  - 深度或突波神經網路FPGA加速器(Deep/Spiked Neural Network FPGA accelerator)

- 類比電路專題：
  - IoT感測器介面設計 (Interface Circuit for IoT Sensors)
  - 生醫晶片關鍵電路 (Bio-signal amplifier, low-power ADC, power regulator, etc.)

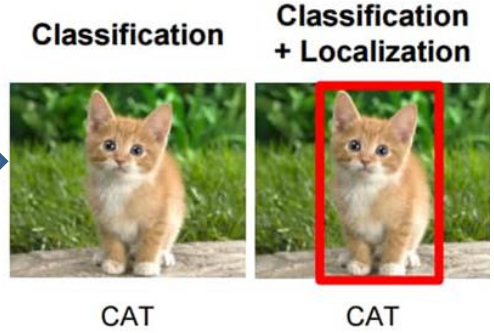
深度/突波神經網路FPGA加速器



Input Image



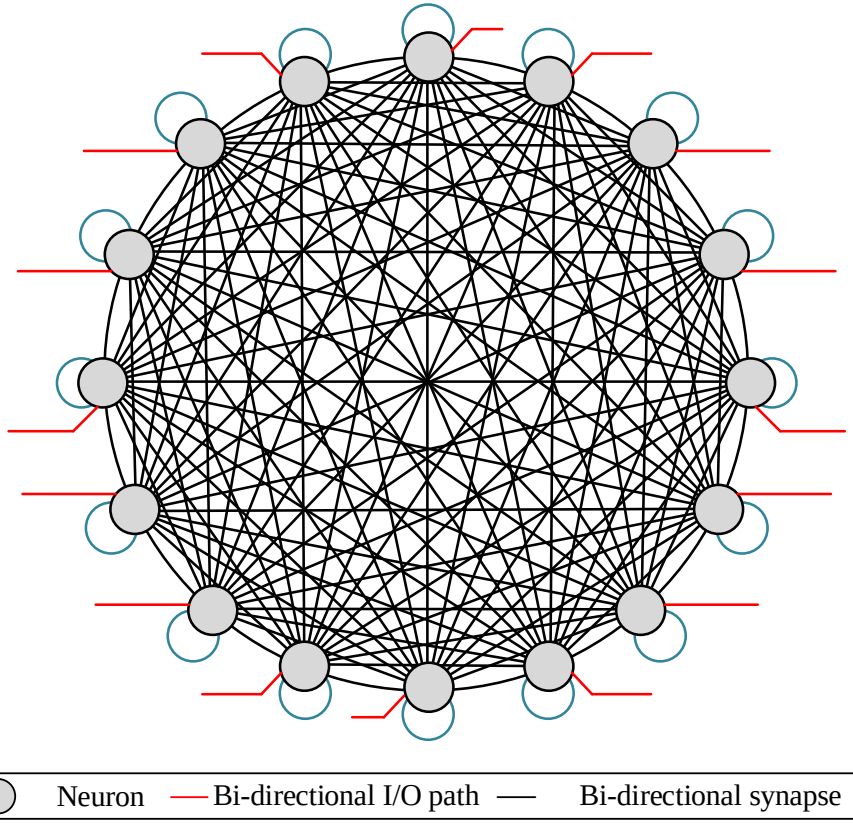
FPGA System

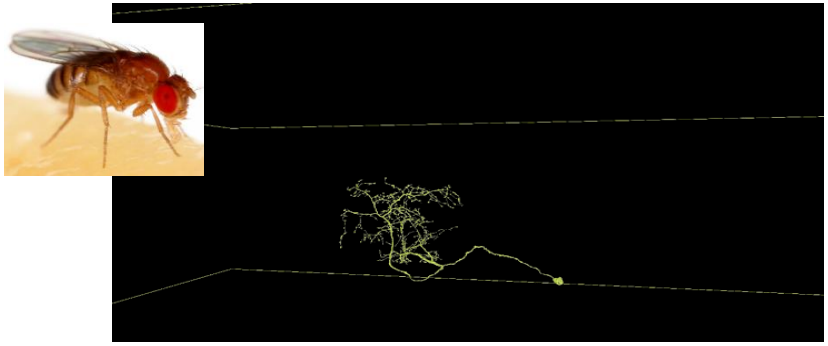


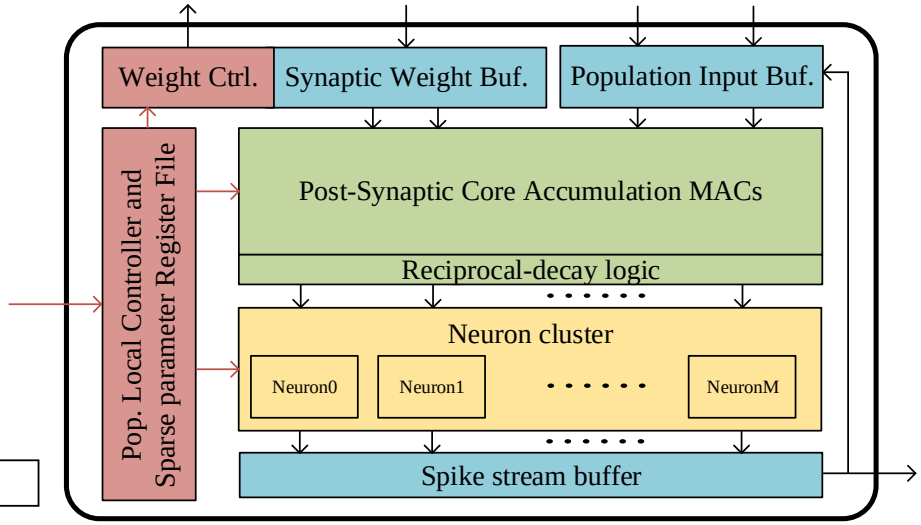
Predict Result

- 此專題將包括系統設計、神經網路實作(CNN, SNN)、FPGA系統實作等。

神經群仿生神經網路處理器

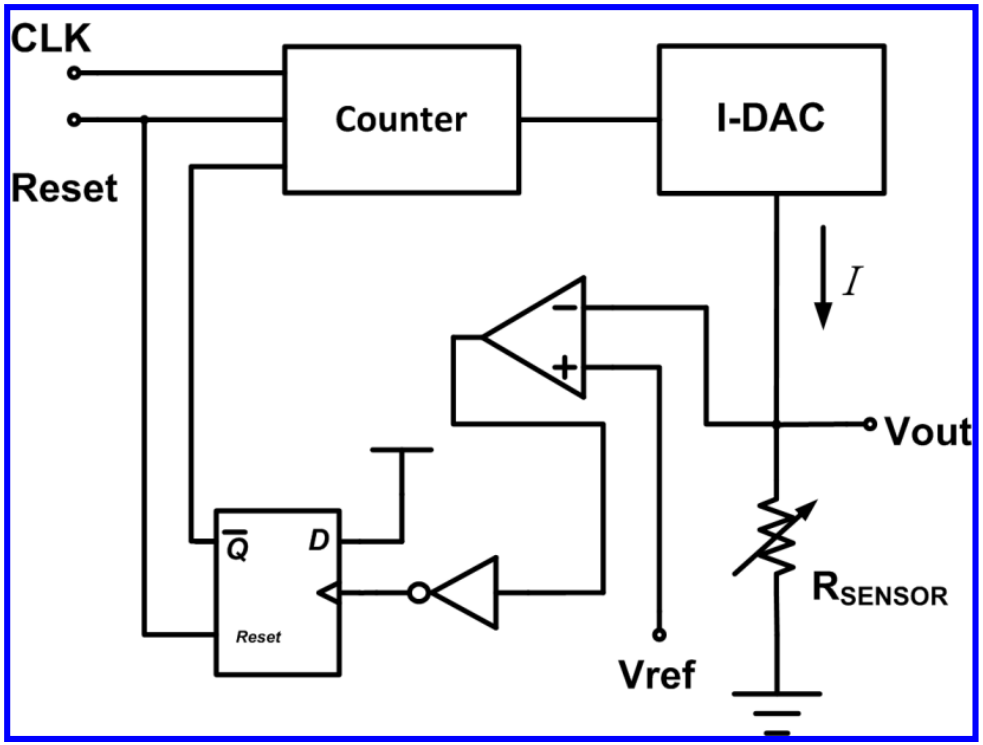


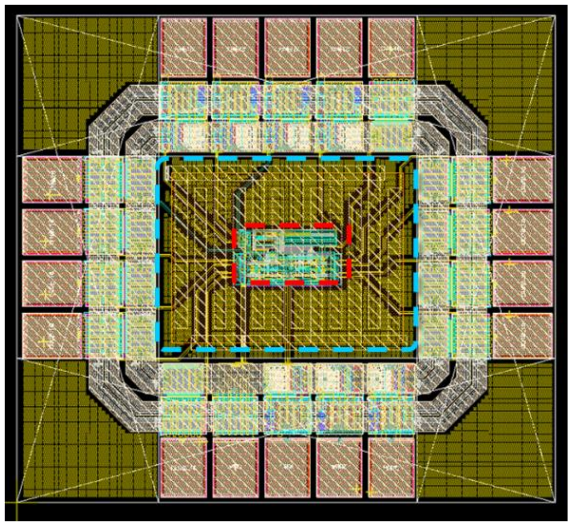




- 從仿生角度出發，此專題將包括突波神經網路設計(SNN)、FPGA系統實作等。

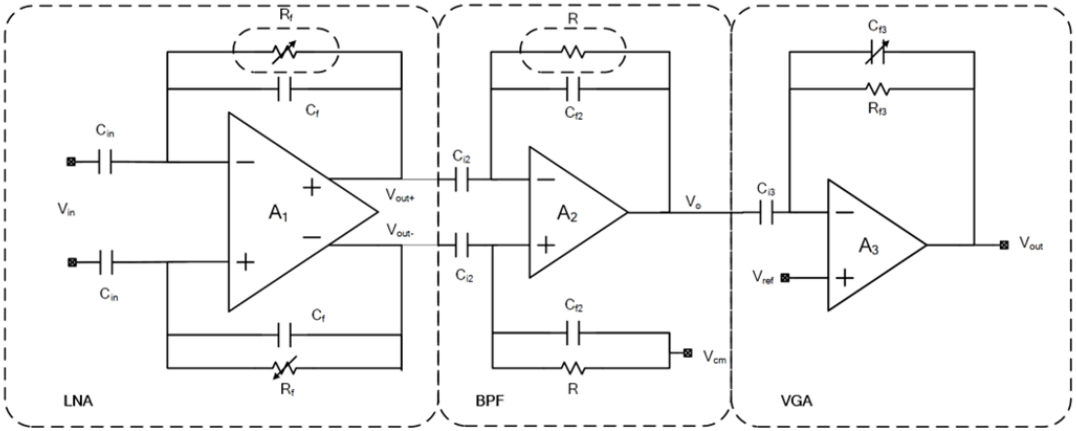
IoT感測器介面設計





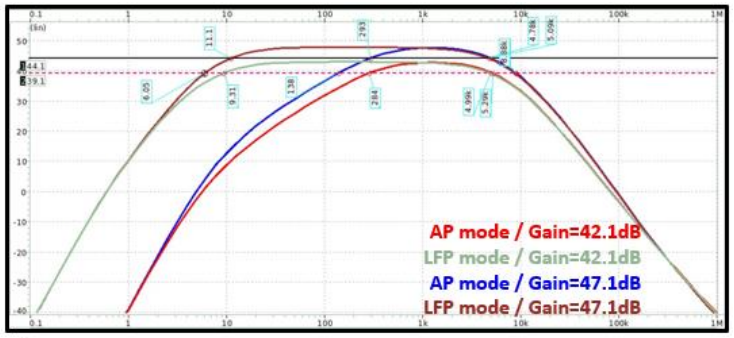
- 此專題將包括感測器、類比介面電路設計流程、加熱器回授控制。本專題將目標於TSRI下線並量測。

A Low-Noise Neural Signal Amplifier with Adjustable Gain and Bandwidth for Capturing AP/LFP Signals Separately



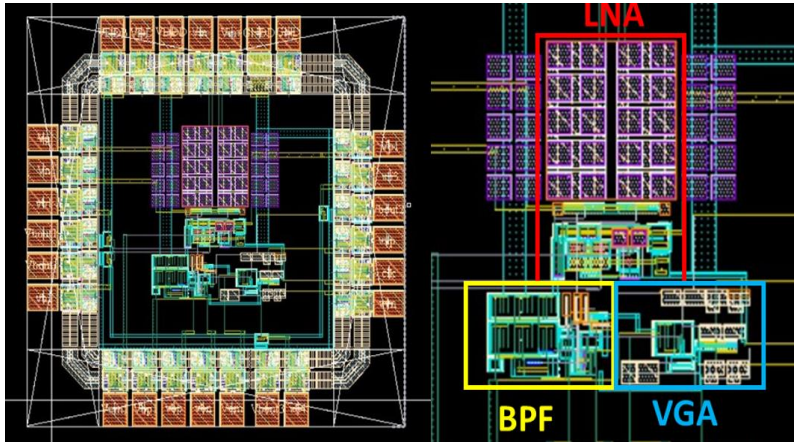
▲ Fig1. Block Diagram of three stage low-noise amplifier.

- ✓ Low Noise, Low Power
- ✓ Adjustable Gain
- ✓ Adjustable Bandwidth (AP/LFP mode)



TT 37℃	spec	Pre-sim	Post-sim	[1]	[3]
Total current(uA)	-	1.60	1.65	3.60	2.82
Gain(dB) Clk=0/Clk=1	>40	47.7 / 42.9	47.1 / 42.1	45 / 55	45/ 63
Bandwidth(Hz) AP/LFP	20-4k / 400-4k	6.5-5.51k / 335-5.94k	10.8-4.56k / 300-5.09k	0.8-4.15k / 300-8.2k	1-0.5k / 800-5.8k
Power(uW)	<6	1.60	1.65	3.60	2.82
Noise (uVrms)	<15	7.17	8.05	2.1	3.6
Supply voltage (V)	1	1	1	1	1
PSRR(dB) AP/LFP	>60	70 / 67	68 / 67	92.48	70
CMRR(dB) AP/LFP	>60	78/70	66.9/65.1	98.28	80

▲ Table1. Performance Table



▲ Fig2. The test chip is fabricated in TSMC 0.18μm CMOS process and the chip size is 0.93 mm^2

Implementation and Improvement of An Automatic Gain Control (AGC) Amplifier for Deep Brain Stimulation

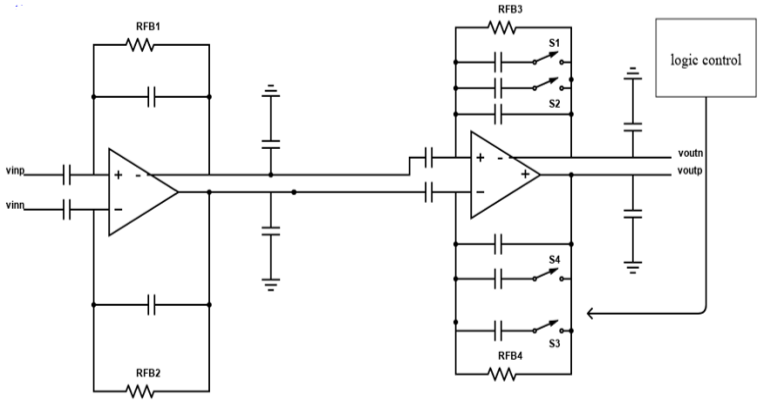


Fig. 1 Block Diagram of the neural recording front-end.

- ✓ Low Noise, Low Power
- ✓ Automatic adjustable Gain (prevent HVS)

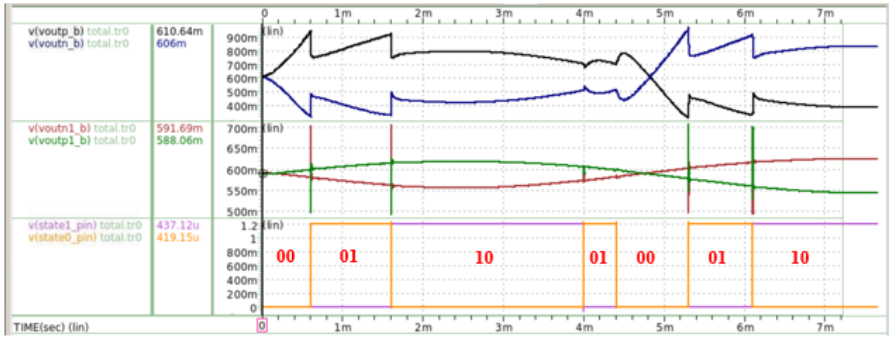


Fig.5 Simulation waveform.

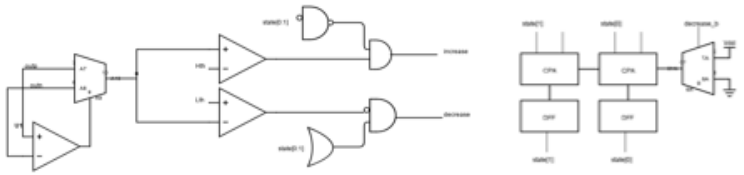


Fig.2 Block diagrams of logic circuits.

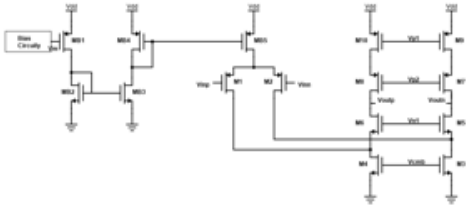


Fig.3 The folded-cascode amplifier used in LNA.

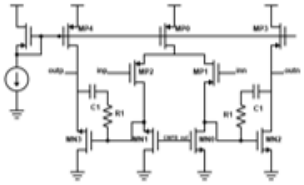
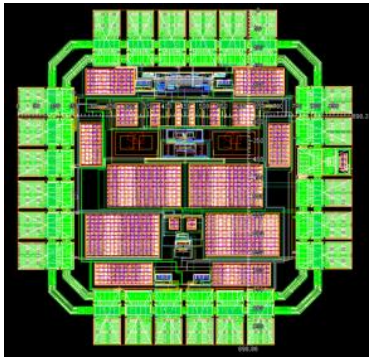


Fig. 4 The two-stage amplifier used in PGA.

Specification	Spec.	This work Pre-sim(TT)
Power Supply(V)	1.2V(Analog)	1.2V(Analog)
Closed-loop Gain (dB)	66	63.3
fL(Hz)/ fH(Hz)	<1.8 / >300	1.46 / 349
IRN(μVrms)	< 5	0.64
Chip size(mm²)	< 0.9 x 0.9	< 0.9 x 0.9

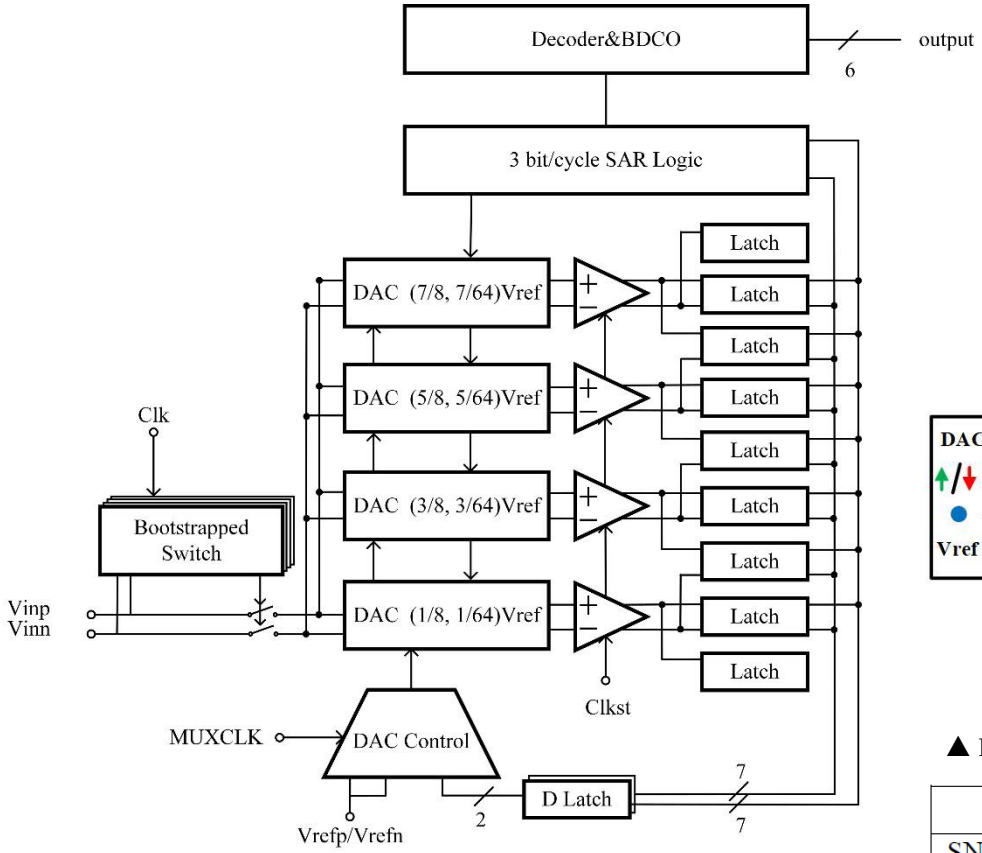
▲ Table1. Performance Table



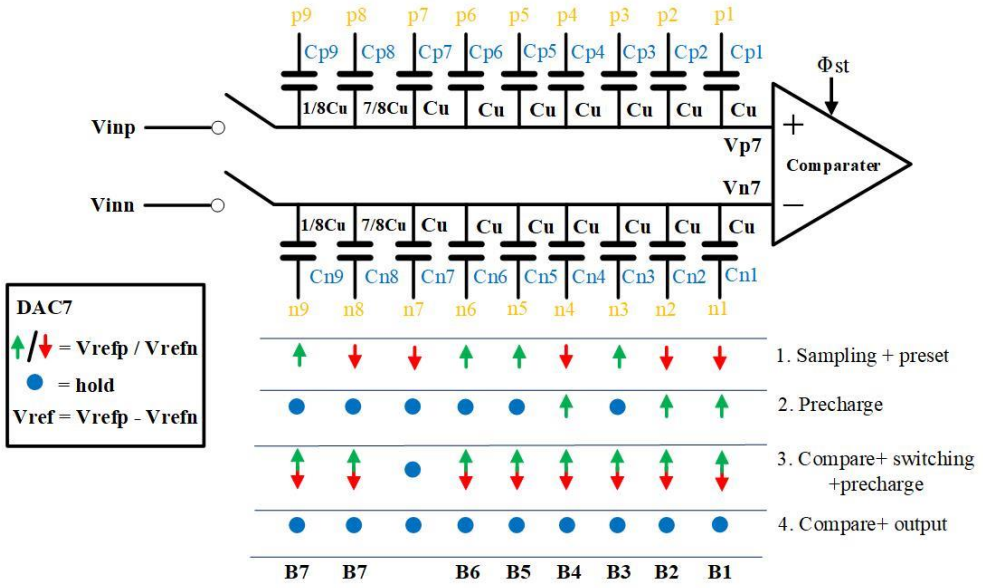
▲ Fig6. The test chip is fabricated in TSMC 90μm CMOS process and the chip size is 0.80 mm^2

A 6 bits 25MS/s 3b/cycle SAR ADC with Boundary Detection Code Overriding (BDCO)

- ✓ SAR + Flash A/D → Speed ↑, Efficiency ↑
- ✓ Interpolation → Comparator Counts ↓
- ✓ BDCO → Accuracy ↑, Power Consumption ↓



▲ Fig1. Block Diagram

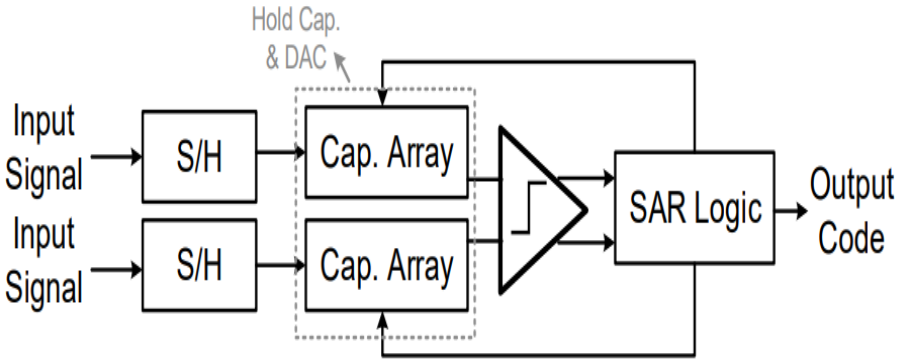


▲ Fig2. Switching Scheme

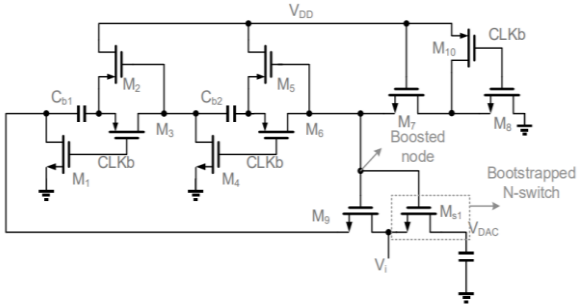
	TT	SS	FF
SNDR(dB)	37.09657	37.17924	36.84520
ENOB(Bits)	5.869862	5.883594	5.828106
SFDR(dB)	49.46530	49.96652	48.79998
Power(mW)	1.2482	1.0483	1.5735

▲ Fig3. Pre-sim Table

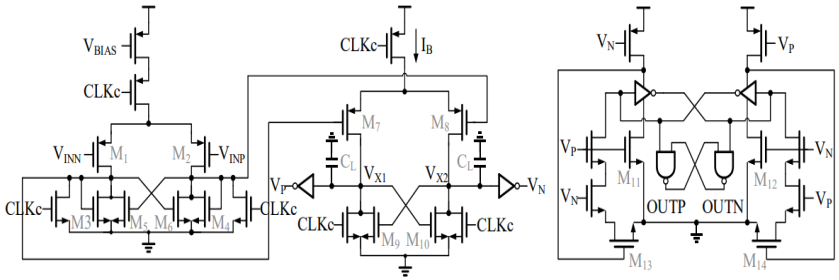
A 10-bit 320kS/s SAR ADC design and application



▲ Fig.1 Block Diagram of SAR ADC

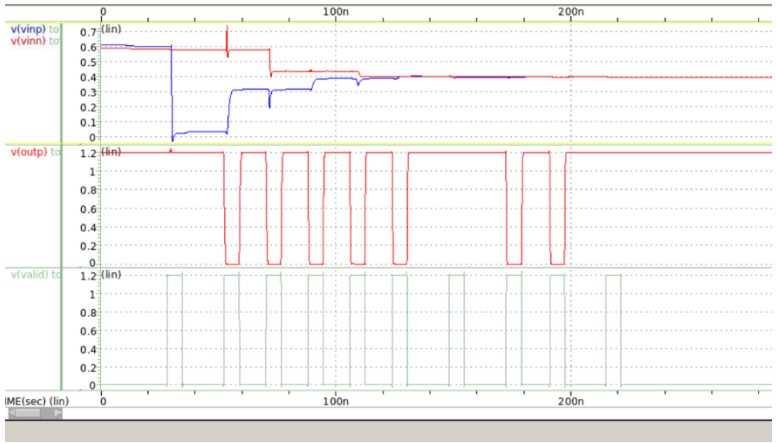


▲ Fig.2 Sample and hold circuit, S/H



▲ Fig.3 Comparator

✓ MSB-2 skip logic → Power Consumption ↓

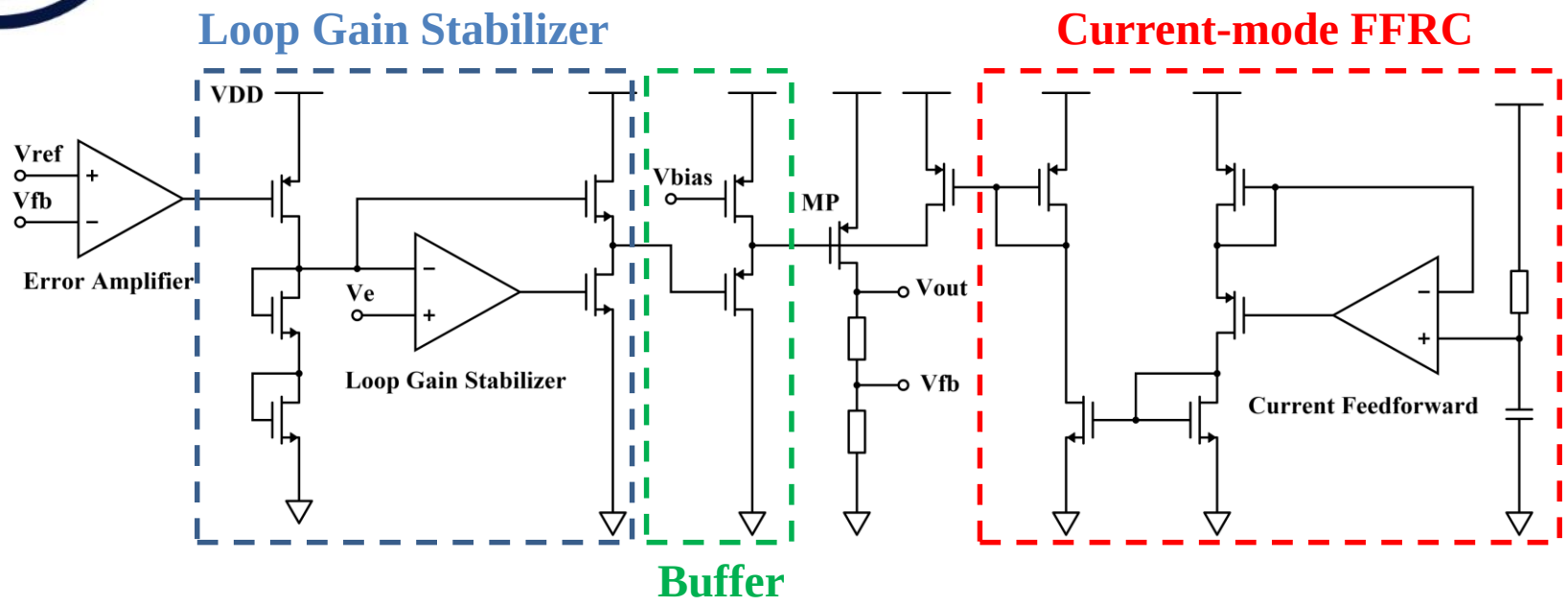


▲ Fig.4 ADC work schematic waveform

Item	Spec	This Work
Supply Voltage	1.2V	1.2V
Sampling Rate	320kS/s	320KS/s
SNDR (dB)	>56(dB)	>58.2(dB)
ENOB	>9bits	9.2bit
Power Consumption	< 5μW	4.82μW

▲ Table1. Performance Table

LDO PSR Enhancement with Current-mode FFRC and Loop Gain Stabilizer



The output of the Error Amplifier (EA) is fixed at Ve

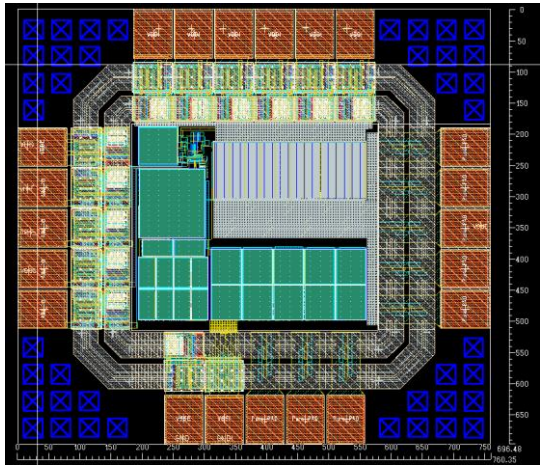
- ✓ Operation point of EA and the loop gain of the LDO is stable

Buffer is added between MP and EA

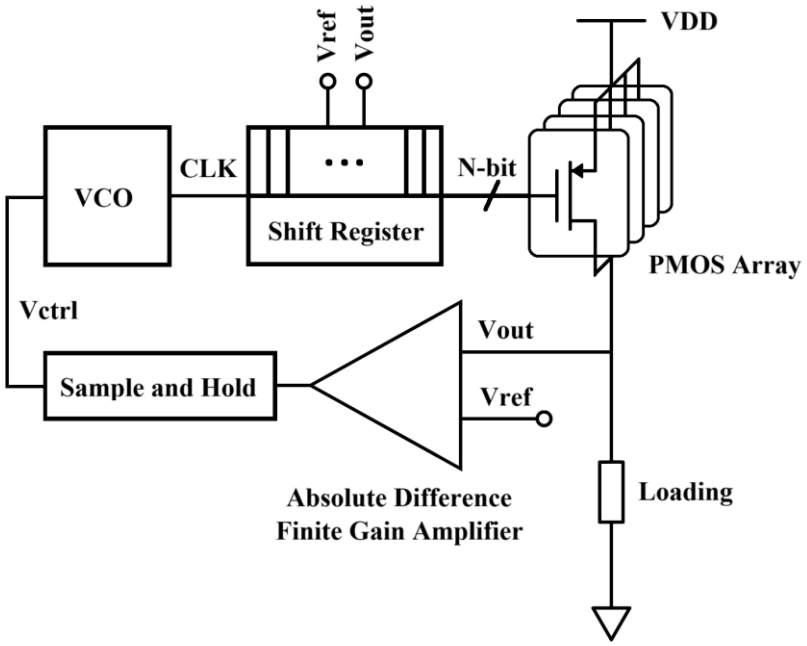
- ✓ High impedance of EA output and high capacitance of MP gate are split

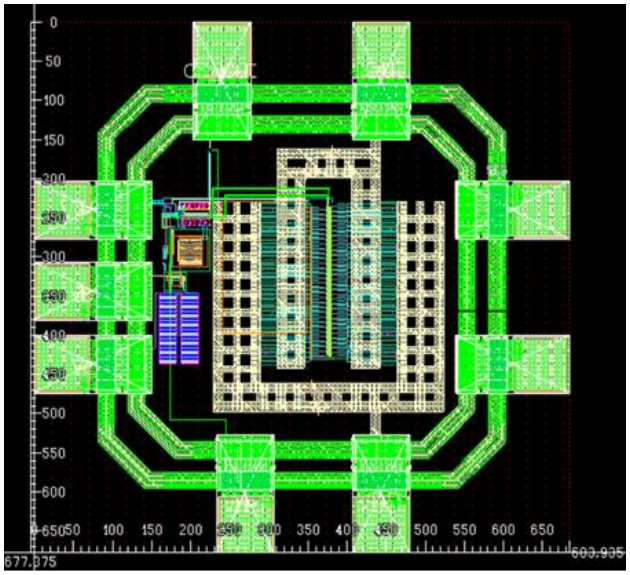
Current-mode feedforward ripple cancellation (FFRC)

- ✓ Power supply noise is cancelled, PSR is enhanced



Digital LDO Transient Response Enhancement with VCO





Nearly all digital architecture

- ✓ Low power supply can be achieved compared to analog LDO

Voltage-controlled oscillator and adaptive clock are used

- ✓ Low quiescent current (I_Q) at steady state
- ✓ High speed clock for fast load transient response

專題說明

- 希望學生具備之背景知識或建議選修課程
  - 電子學(實驗)、電路學(實驗)、邏輯設計(實驗)、程式設計、Verilog、FPGA、AIC、VLSI、IC Lab等
- 進行方式: 每週與老師與研究生討論
- 希望人數／組: 2-3人
- 可接受組數: 各1-2組
- 會學到的技術:系統考量與設計、雛型實作、電路設計、電路板或晶片製作、軟體撰寫
- 面談資料: 成績單、組員、有興趣之題目
- 有問題可直接寫信討論
  - kttang@ee.nthu.edu.tw